## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for verifying a generated computer code having a plurality of lines generated from a model file of a system comprising:

processing the model file to determine an expected computer code having a plurality of lines based on the model file;

comparing the generated computer code to the expected computer code to determine if the generated computer code and the expected computer code match; and

transmitting an error message if the generated computer code and the expected computer code do not match.

2. (Previously Presented) The method of claim 1 further, comprising the steps of:

comparing each of the lines of the generated computer code to an expected form to verify each of the lines of the generated computer code is in a proper format; and

transmitting the error message if the generated computer code is not in the proper format.

3. (Previously Presented) The method of claim 1, further comprising the steps of:

comparing the generated computer code to the expected computer code to determine if the generated computer code includes any line of code not in the expected computer code; and

transmitting the error message if the generated computer code includes any line of code not in the expected computer code.

4. (Previously Presented) The method of claim 1, further comprising the steps of:

comparing the generated computer code to the expected computer code to determine if the lines of the generated computer code are in a logical order; and

transmitting the error message if the lines of the generated computer code are not in logical order.

5. (Previously Presented) The method of claim 1, further comprising the steps of:

comparing a header information section of the generated computer code to an expected header information section to determine if the header information section of the generated computer code matches the expected header information; and

transmitting the error message if the header information section of the generated computer code does not match the expected header information.

6. (Previously Presented) The method of claim 1, further comprising the steps of:

comparing a generated declared variable section of the generated computer code to an expected declared variable section of an expected computer code to determine if the generated declared variables section matches the expected declared variable section; and

transmitting the error message if the generated declared variables section does not match the expected declared variable section.

7. (Currently Amended) A computer-readable storage medium containing a set of instructions for verifying a generated computer code having a plurality of lines, the generated computer code automatically generated from a model file of a system, the set of instructions comprising:

code that reads in [[a]] the model file;

code that determines an expected computer code having a plurality of lines based on the model file;

code that reads in the generated computer code;

code that compares the generated computer code to the expected computer code to determine if the generated computer code and the expected computer code match; and

code that transmits an error message if the generated computer code and the expected computer code do not match.

8. (Previously Presented) The medium of claim 7, wherein the set of instructions further comprises:

code that compares each of the lines of the generated computer code to an expected form; and

code that transmits the error message if the generated computer code does not include all of the lines of the expected computer code.

9. (Previously Presented) The medium of claim 7, wherein the set of instructions further comprises:

code that compares the generated computer code to the expected computer code to determine if the generated computer code includes any line of code not in the expected computer code; and

code that transmits the error message if the generated computer code includes any line of code not in the expected computer code.

10. (Previously Presented) The medium of claim 7, wherein the set of instructions further comprises:

code that compares the generated computer code to the expected computer code to determine if the lines of the generated computer code are in a logical order; and

code that transmits the error message if the lines of the generated computer code are not in logical order.

11. (Previously Presented) The medium of claim 7, wherein the set of instructions further comprises:

code that compares a header information section of the generated computer code to an expected header information section to determine if the header information section of the generated computer code matches the expected header information; and

code that transmits the error message if the header information section of the generated computer code does not match the expected header information.

12. (Currently Amended) A system for verifying the contents of a generated computer code generated from a model file, comprising:

a processor operable to compare the generated computer code with an expected computer code and transmit an error message if the generated computer code and the expected computer code do not match, the expected computer code generated by the processor based on the model file; and

a display configured to display the error message coupled to the processor.

13. (Previously Presented) The system of claim 12 wherein the error message indicates if the generated computer code has all of the content of the expected computer code.

14. (Previously Presented) The system of claim 12 wherein the error message indicates if the generated computer code has any additional content not found in the expected computer code.

15. (Previously Presented) The system of claim 12 wherein the processor is operable to compare each of the lines of code in the generated computer code to an expected form and transmit the error message if each of the lines of code in the generated computer code do not match the expected form.

16. (Previously Presented) The system of claim 12 wherein the processor is operable to compare the generated computer code to the expected computer code to determine if the generated computer code includes any line of code not in the expected computer code and transmit the error message if any lines of code in the generated computer code is not in the expected computer code.

17. (Previously Presented) The system of claim 12 wherein the processor is operable to compare the generated computer code to the expected computer code to determine if the lines of the generated computer code are in a logical order and transmit the error message if the lines of the generated computer code are not in logical order.

18. (Previously Presented) The system of claim 12 wherein the processor is operable to compare a header information section of the generated computer code to an expected header information section to determine if the header information section of the generated computer code matches the expected header information and transmit the error message if the header information section of the generated computer code does not match the expected header information.

19-20. (Canceled)

21. (Previously Presented) The method of claim 1, further comprising the steps of: comparing the generated computer code to the expected computer code to determine if the generated computer code includes all of the lines of the expected computer code; and

transmitting an error message if the generated computer code does not include all of the lines of the expected computer code.

22. (Previously Presented) The medium of claim 7, wherein the set of instructions further comprises:

code that compares the generated computer code to the expected computer code to determine if the generated computer code includes all the lines of the expected computer code; and

code that transmits the error message if the generated computer code does not include all of the lines of the expected computer code.